REMARKS

The Office Action dated May 21, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. By this Amendment, claims 3, 13 and 19 have been cancelled. The subject matter of claims 3 and 13 has been incorporated into claims 4 and 14, respectively. Therefore, claims 4 and 14 are now in independent form. Claims 1, 5, 7 8, 9 10, 11, 15, 18 and 20 have been further amended to more clearly particularly point out and distinctly claim the invention. No new matter has been added. Accordingly, claims 1, 2, 4-12, 14-18 and 20 are pending in this application and are submitted for consideration.

Applicant acknowledges and thanks the Examiner for indicating that claims 12 and 17 are allowed over the prior art and that claims 4, 6, 14 and 16 would be allowable over the prior art if amended to be in independent form. By this Amendment, claims 4 and 14 have been written in independent form. Therefore, Applicant submits that these claims are also in condition for allowance. However, Applicant respectfully submits that claims 6 and 16 recite allowable subject matter and therefore, placing them into independent form is not necessary.

Claims 18 and 20 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claim 18 is generally explained in Reference to Fig. 3. The phrase "having pulses" refers to, for example, "PLSH" and "PLSL" under (2):typ. With respect to claim 20, for example in Fig. 3, the "PLSH" and the "PLSL," under (2):typ do not overlap each other, and thus, generate two PORs.

Therefore, Applicant respectfully requests that the rejection be withdrawn.

Claims 1, 2, 7 and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Zhou, et al. (U.S. Patent No. 6,362,669, "Zhou"). However, Applicant respectfully submits that claims 1, 2, 7 and 10 recite subject matter that is neither disclosed nor suggested in the prior art.

Applicant's amended claim 1 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other. A main reset signal generator is provided for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.

Applicant's amended claim 7 recites a method of initializing a semiconductor integrated circuit comprising the steps of: generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other, and independently of each other, at least one of the pulse signals including a rectangular pulse; and initializing an internal circuit according to at least one from any of the power-on reset signals.

Applicant's amended claim 10 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other. A plurality of pulse generators generate pulses on the basis of the plurality of sub power-on reset signals, respectively, at least one of said pulses being a rectangular pulse. A composite circuit synthesizes the pulses to generate a main power-on reset signal.

Zhou discloses a power-on reset circuit that delays de-assertion of a POR control signal in an IC device. When unstable power levels are detected, the POR control signal is maintained in an asserted condition until the IC device is fully reset. As shown in Fig. 5, POR circuit 500 includes a one-shot delay circuit 520 and a power-up delay circuit 530 connected in parallel between detection 120 and NOR gate 540. Inverter 550 is connected to the output terminal of NOR gate 540, and generates control signal POR. One-shot delay circuit 520 includes first inverter 522 is connected to an output terminal of detector circuit 120, detector circuit 120 generates detection signal POR1. A lock circuit 524 having a first input terminal connected to the output terminal of inverter 522, and a one-shot circuit 526 having an input terminal connected to the output terminal of lock circuit 524.

Power-up delay circuit 530 includes two or more series-connected inverters 532 and 534. Inverts 532 and 534 delay the transmission of high-to-low changes of detection signal POR1 for a longer delay period than low-to-high changes.

However, in Zhou, the plurality of sub power-on reset signals are dependent on each other because they are generated based on the same signal. In contrast, in Applicant's present invention, the plurality of sub power-on reset signals are generated independently of each other, as recited in Amended Claims 1, 7 and 10.

Therefore, in Zhou, if there is no initial signal generated, the internal circuit cannot be reset. But, in the present invention, even if one of the sub power-on reset signals does not generate for some reason, the other sub power-on reset signals can accurately reset the internal circuit.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 1, 7 and 10, is not anticipated within the meaning of 35 U.S.C. § 102.

As claim 2 depends from claim 1, Applicant respectfully submit that this claim incorporates the patentable aspects thereof, and are therefore allowable for at least same reasons as discussed above.

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by Lee (U.S. Patent No. 6,492,848,"Lee").

As will be discussed below, Applicant respectfully submits that claim 1 recites subject matter that is neither disclosed nor suggested by the prior art.

Lee discloses a power-on reset for generating reset signals for different power on signals, as shown Fig. 4, unit 410, Schmitt trigger inverter430 and reset generator 450. Input unit 410 receives a power-on signal from an external circuit and produces an internal circuit. Schmitt trigger inverter 430 receives the internal power-on signal and produces an inverted signal. Reset generator 450 produces a power-on reset signal (POR) in response to the output of Schmitt trigger inverter 430.

However, in Lee, the plurality of sub power-on reset signals are dependent on each other because they are generated based on the same signal. In contrast, in Applicant's present invention, the plurality of sub power-on reset signals are generated independently of each other, as recited in Amended Claim 1.

Therefore, in Lee, if there is no initial signal generated, the internal circuit cannot be reset. But, in the present invention, even if one of the sub power-on reset signals does not generate for some reason, the other sub power-on reset signals can accurately reset the internal circuit.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claim 1, is not anticipated within the meaning of 35 U.S.C. § 102.

Claims 8, 9, 11, 18, and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhou. In making this rejection, the Office Action took the position that Zhou discloses all the elements of the claimed invention, except for disclosing the generation of signals on the basis of respective threshold valued of the transistors.

Applicant's amended claim 8 recites a semiconductor integrated circuit having a plurality of sub reset signal generators, including transistors having threshold values, for generating a plurality of sub power-on reset signals on basis of the respective threshold values of each of the transistors, and independently of each other. A main reset signal generator is provided for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit according to at least one of the sub power-on reset signals.

Applicant's amended claim 9 recites a semiconductor integrated circuit including a first sub reset signal generator, having a first transistor having a first threshold value, for generating a first sub power-on reset signal on basis of the first threshold value. A second sub reset signal generator, including a second transistor having a second threshold value, is provided for generating a second sub power-on reset signal on basis of the second threshold value, independently of the first sub reset signal generator. A main reset signal generator is provided for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of the first sub power-on reset signal and the second sub power-on reset signal.

Applicant's amended claim 11 recites a method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of: generating a plurality of sub power-on reset signals, according to respective threshold values of each of the transistors, and independently of each other; generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, at least one of said pulse signals including a rectangular pulse; and initializing an internal circuit according to at least one of said power-on reset signals.

Applicants amended claim 18 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other. A main reset signal generator is provided for generating a main power-on reset signal to initialize an internal circuit, according to at least one of the plurality of sub power-on reset signals. The main reset signal generator generates the main power-on reset signal having pulses respectively corresponding to each of the sub power-on reset signals, when threshold values of transistors formed in the semiconductor integrated circuit are typical values.

Applicant's amended claim 20 recites a method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of: generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors, and independently of each other; generating a plurality of pulse signals

as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, the power-on reset signals having pulses not overlapping each other when threshold values of transistors formed in the semiconductor integrated circuit are typical values; and initializing an internal circuit according to at least one of the pulses of the power-on reset signals.

With respect to claim 8, the Office Action took the position that it would have been obvious to form each of the inverters as a CMOS inverter, and each of the logic devices using appropriate combinations of MOS transistors.

With respect to claim 11, the Office Action took the position that it would have been obvious to use CMOS inverters for each of the inverts of Zhou.

With respect to claim 9, the Office Action took the position that with respect to Fig. 6(f) of Zhou, the main reset signal generator 540, 550 generates pulse signal POR.

With respect to claim 18, the Office Action took the position that transistors are well-known means for forming inverters.

With respect to claim 20, the Office Action took the position that it would have been obvious to use transistors within the inverters of Zhou.

However, firstly, the Office Action has failed to provide motivation as to why one of ordinary skill in the art would be compelled to make the suggested modifications.

Secondly, in Zhou, the plurality of sub power-on reset signals are dependent on each other because they are generated based on the same signal. In contrast, in Applicant's present invention, the plurality of sub power-on reset signals are generated independently of each other, as recited in Amended Claims 8, 9, 11, 18 and 20.

Therefore, in Zhou, if there is no initial signal generated, the internal circuit cannot be reset. But, in the present invention, even if one of the sub power-on reset signals does not generate for some reason, the other sub power-on reset signals can accurately reset the internal circuit.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 8, 9, 11, 18 and 20 is not obvious within the meaning of 35 U.S.C. § 103.

Claims 8, 9 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee. In making this rejection, the Office Action took the position that Lee discloses all the elements of the claimed invention, with the exception of disclosing the generation of signals to initiate an internal circuit.

As discussed above, in Lee, the plurality of sub power-on reset signals are dependent on each other because they are generated based on the same signal. In contrast, in Applicant's present invention, the plurality of sub power-on reset signals are generated independently of each other, as recited in Amended Claims 8, 9 and 18.

Therefore, in Lee, if there is no initial signal generated, the internal circuit cannot be reset. But, in the present invention, even if one of the sub power-on reset signals does not generate for some reason, the other sub power-on reset signals can accurately reset the internal circuit.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 8, 9 and 18, is not obvious within the meaning of 35 U.S.C. § 103.

Claims 3, 5, 13, 15 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhou in view of Lee. In making this rejection, the Office Action took

the position that Zhou discloses all the elements of the claimed invention. Lee is cited for curing the deficiencies of Zhou.

By this Amendment, Claims 3, 13, 19 have been cancelled. Therefore, the rejection is moot. However, the Applicant submits that claims 5 and 15 recite subject mater that is neither taught nor suggested in any combination of the prior art.

Applicant's amended claim 5 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other. A reset terminal is provided for receiving an external power-on reset signal. A main reset signal generator is provided for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of the sub power-on reset signals and the external power-on reset signal.

Applicant's amended claim 15 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other. A reset terminal is provided for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit. A main reset signal generator is provided for generating a rectangular pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of the sub power-on reset signals and the external power-on reset signal.

The Office Action asserted that it would have been obvious to one of ordinary skill in the art to modify Zhou by incorporating an external power-on reset signal in order to reset the circuit without powering down.

As discussed above, neither Zhou nor Lee, either alone or in combination, discloses or suggests the claimed invention.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 5 and 15, is not obvious within the meaning of 35 U.S.C. § 103.

Claims 13 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malherbe in view of Lee. In making this rejection, the Office Action took the position that Malherbe discloses all the elements of the claimed invention, except for disclosing an external power-on reset signal supplied from the exterior. Lee is cited for teaching this limitation. By this Amendment, claim 13 has been cancelled. Therefore, the rejection is moot. However, Applicant submits that claim 15 recites subject matter that is neither taught nor suggest in any combination of the prior art.

The Office Action took the position that it would have been obvious to one of ordinary skill in the art to include a reset terminal as a means to provide an external reset signal in Malherbe, for the purpose of resetting the circuit without powering.

However, as discussed above, Lee fails to disclose or suggest the claimed invention. Thus, neither Malherbe nor Lee, either alone or in combination, discloses or suggests the claimed invention.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claim 15 is not obvious within the meaning of 35 U.S.C. § 103.

Claims 13 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Crotty in view of Lee. In making this rejection, the Office Action took the position that Crotty discloses all the elements of the claimed invention, except for disclosing a reset terminal for receiving an external power-on signal. Lee is cited for teaching this limitation. By this amendment, claim 13 has been cancelled. Therefore, the rejection is moot. However, Applicant submits that claim 15 recites subject matter that is neither taught nor suggest in any combination of the prior art.

The Office Action took the position that it would have been obvious to one of ordinary skill in the art to include a reset terminal in the circuit of Crotty in order to reset the circuit without powering down the system.

However, as discussed above, Lee fails to disclose or suggest the claimed invention. Thus, the neither Crotty nor Lee, either alone or in combination, discloses or suggests the claimed invention.

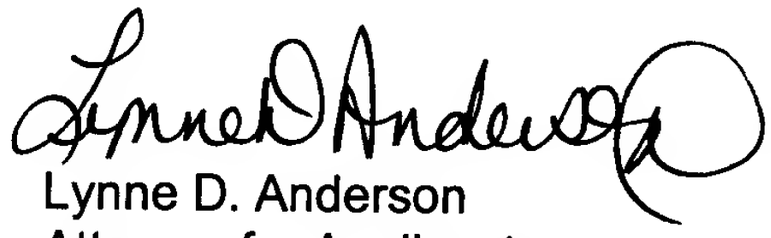
Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 13 and 15, is not obvious within the meaning of 35 U.S.C. § 103.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1, 2, 4-12, 14-18 and 20, and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00025.**

Respectfully submitted,



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